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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/632,024 | 07/31/2003 | Gerard Chauvel | TI-35461 (1962-05418) | 9347 |

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| EXAMINER | |
|---|---|
| SWEARINGEN, JEFFREY R | |
| **ART UNIT** | **PAPER NUMBER** |
| 2145 | |

| NOTIFICATION DATE | DELIVERY MODE |
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| 08/22/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/632,024 | CHAUVEL ET AL. | |
| | Examiner | Art Unit | |
| | Jeffrey R. Swearingen | 2145 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. This case has been reassigned to a new Examiner.

### *Response to Arguments*

2. Applicant's arguments filed 7/11/07 have been fully considered but they are not persuasive.

3. Applicant argues that Evoy failed to disclose *a wait unit coupled to said first and second processor, said wait unit detects said pre-determined address and asserts a wait signal to cause said first first processor to enter a wait mode.* Applicant admits Evoy enters a reduced power state based upon determining that a Java application needs to be executed. Applicant's pre-determined address determination acts as a hardware trap based upon the reading of paragraph 0019 of the originally filed specification. One of ordinary skill in the art is aware that trap functions are commonly invoked by using a command to a "predetermined address" in memory holding the assembly level code of the trap commands. Evoy gives support for this interpretation in column 4, lines 49-50 which list the Java instructions Loads, Stores, Computation, Branch, Push, and Field, which are all commonly known assembly level commands that function as traps.

4. Referring to column 6, lines 7-23, the invocation of a Java application generates a Java mode signal. The previous cited portion of Evoy in column 4 allows branch and load instructions to be part of this step. The assembly level detection of one of these commands "at a predetermined address" would therefore trigger the wait signal changing the power mode. Evoy is allegedly silent on this issue because the underlying principle of a trap being called from an address is taught in introductory computer organization classes for undergraduate students in computer engineering and computer science. One of ordinary skill in the art is well aware of the basic functions of a computer on the assembly language and operating system level.

5. Applicant argues Miller failed to teach *a decode logic unit that determines when a first processor runs a transaction to a pre-determined address...wherein said logic asserts a signal propagated by the first processor interface to cause said first processor to stall.* Miller does wait for a signal contrary to Applicant's assertion. See Miller, column 10, lines 39-45. The processor P1 waits for the clearing of the

availability bit, which is a signal. Applicant never claimed the use of a *completion signal*, contrary to Applicant's arguments.

6. Applicant failed to address the Shenk reference.

7. Applicant failed to address the Mustafa reference.

8. Applicant failed to address the Johnson reference.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-3, 7, 9-10, 12, 21 and 24 rejected under 35 U.S.C. 102(e) as being anticipated by Evoy et al. (US 6,766,460).

11. In regard to claim 1, Evoy taught a system, comprising: a first processor that executes a transaction targeting a pre-determined address (column 6, lines 15-30, where a host processor initiates a Java application, thus informing the power management system, seen as a predetermined address); a second processor coupled to said first processor (Figure 1, with the master processor and the slave processor both coupled to the system bus); and a wait unit coupled to said first and second processors, said wait unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a wait mode (column 6, lines 15-35, where the power managemnet system detects the transaction to the Java processor, seen as a predetermined address, and subsequently signals the host process to power down, seen as a wait state.)

12. In regard to claim 2, Evoy taught the wait signal is de-asserted to permit the first processor to retrieve a status of the second processor (column 6, line 62 - column 7, line 10, where the Java completion signal is sent to bring the host processor out of its wait sate and therefore the host processor retrieves completion status of the Java processor simply by receiving the Java completion signal).

13. In regard to claim 3, Evoy taught the status includes one or more instructions that the first processor is to execute (column 10, line 65 – column 11, line 17)

14. In regard to claim 7, Evoy taught said wait unit de-asserts the wait signal upon detection of a signal from said second process (column 7, lines 4-7)

15. In regard to claim 9, Evoy taught executing a transaction that targets a predetermined address (column 6, lines 15-30); detecting the transaction to said pre-determined address; asserting a wait signal upon detection of the transaction to cause a processor to stall (column 6, lines 15-35); causing said wait signal to de-assert upon occurrence of an event (column 6, lines 62 – column 7, lines 10), said de-assert controlled by logic external to said processor (column 7, lines 4-10).

16. In regard to claim 10, Evoy taught said stall comprises a low power mode (column 6, lines 23-27).

17. In regard to claim 12, Evoy taught said event comprises a signal from another processor (column 6, line 62 – column 7, line 7)

18. In regard to claim 21, Evoy taught a first processor; a second processor; means for detecting a transaction targeting a pre-determined address (column 6, lines 15-30) and for asserting a wait signal ot said first processor to cause the first processor to enter a wait state (column 6, lines 15-35); and means for releasing said first processor from the wait state (column 6, line 62 – column 7, line 10).

19. In regard to claim 24, Evoy taught a wait release signal from said said second processor coupled to a wait unit, said wait unit de-asserts the wait signal upon detection of the wait release signal (column 7, lines 4-10).

20. Claims 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller et al. (US 5,596,759).

21. In regard to claim 15, Miller taught a wait unit, comprising: a decode logic unit that determines when a first processor runs a transaction to a pre-determined address (column 5, line 57 – column 6, line

5); a first processor interface; a second processor interface (Figure 1); logic coupled to the decode logic unit, the first processor interface, and the second processor interface, wherein said logic asserts a signal propagated by the first processor interface to cause said processor to stall (column 10, lines 12-45).

22. In regard to claim 18, Miller taught said second processor interface receives a wait release signal from a second processor that causes the wait unit to de-assert the wait signal to said first processor through said first processor interface (column 9, lines 4-53).

***Claim Rejections - 35 USC § 103***

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 4-5, 13-14, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of Shenk (US 4,535,404).

25. In regard to claims 4-5, 13-14, and 22-23, Evoy taught all of the above limitations. Evoy failed to disclose transactions comprising a memory read or a memory write to or from the predetermined address. The concept of reading or writing to memory in order to activate certain principles is known in the art as illustrated by Shenk. Shenk disclosed a system of memory mapped I/O. Memory mapped I/O allows for peripheral devices to be controlled by referencing memory with normal program instructions and the memory is set aside by a predetermined amount of space and addressing within this space (column 1, lines 13-50). It would have been obvious to one of ordinary skill in the art to modify Evoy with memory mapped I/O in order to increase I/O programming flexibility as taught in Shenk, column 1, lines 50-52.

26. Claims 6, 11, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of Mustafa (US 6,678,830).

27. In regard to claims 6, 11 and 25, Evoy disclosed all of the above limitations. Evoy failed to disclose waking the first processor (de-asserting the wait signal) in response to a system interrupt.

Activating processors from a sleep state in response to a system wide interrupt is well known in the art. See Mustafa, column 2, lines 5-30, with a keyboard controller activating computers. The activation is used as an interrupt, and is interpreted as a system interrupt because it can activate the processor from an I/O device. It would have been obvious to one of ordinary skill in the art to modify Evoy with a system interrupt to take advantage of power management functionalities as suggested by Mustafa, column 1, lines 39-41.

28. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Evoy in view of Johnson, Jr. et al. (US 4,420,806).

29. In regard to claim 8, Evoy disclosed all of the above limitations. Evoy failed to disclose having the wait unit, upon detection of a signal, assert a processor interrupt signal to the first processor if the wait signal is already de-asserted. Johnson taught interprocessor interrupts are employed when a processor requires the services of another processor. When the wait unit detects that the wait signal is deasserted, it can only happen from a system interrupt, such as generated by external I/O. If the first processor is active and the second processor needs the first processor, the second processor can produce an interprocessor interrupt as taught in Johnson to request the first processor to execute the tasks which the second processor needs executed. (Johnson, column 1, lines 17-26). It would have been obvious to one of ordinary skill in the art to add interprocessor interrupts to Evoy as taught in Johnson to facilitate implementation of multiple processors to increase speed and reduce size of components as taught in Johnson, column 1, lines 11-17.

30. Claims 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Shenk.

31. In regard to claims 16-17, Miller disclosed all of the above limitations. Miller failed to disclose the transactions comprise a memory read or a memory write to or from the predetermined address. Reading or writing to a memory is well known in the art as shown in Shenk. Shenk disclosed a system of memory mapped I/O. Memory mapped I/O allows for peripheral devices to be controlled by referencing memory with normal program instructions and the memory is set aside by a predetermined amount of space and addressing within this space (column 1, lines 13-50). It would have been obvious to one of ordinary skill

in the art to modify Miller with memory mapped I/O in order to increase I/O programming flexibility as taught in Shenk, column 1, lines 50-52.

32. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Johnson.

33. In regard to claim 19, Miller failed to disclose having the wait unit, upon detection of a signal, assert a processor interrupt signal to the first processor if the wait signal is already de-asserted. Johnson taught interprocessor interrupts are employed when a processor requires the services of another processor. When the wait unit detects that the wait signal is deasserted, it can only happen from a system interrupt, such as generated by external I/O. If the first processor is active and the second processor needs the first processor, the second processor can produce an interprocessor interrupt as taught in Johnson to request the first processor to execute the tasks which the second processor needs executed. (Johnson, column 1, lines 17-26). It would have been obvious to one of ordinary skill in the art to add interprocessor interrupts to Miller as taught in Johnson to facilitate implementation of multiple processors to increase speed and reduce size of components as taught in Johnson, column 1, lines 11-17.

***Conclusion***

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Qiu, Xiaogang et al. "Tolerating Late Memory Traps in ILP Processors." Proceedings of the 26th Annual International Symposium on Computer Architecture. IEEE Computer Society. May 1999. pp 76-87.

Hansen, Per Brinch. Operating System Principles. Prentice-Hall, Inc. January 1973. 384 pages.

| | |
|---|---|
| Chesson et al. | US 5,524,250 |
| Conder et al. | US 5,724,564 |
| Bitar et al. | US 5,872,963 |

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. Swearingen whose telephone number is (571) 272-3921. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jason Cardone can be reached on 571-272-3933. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jason Cardone
Supervisory Patent Examiner
Art Unit 2145

JRS